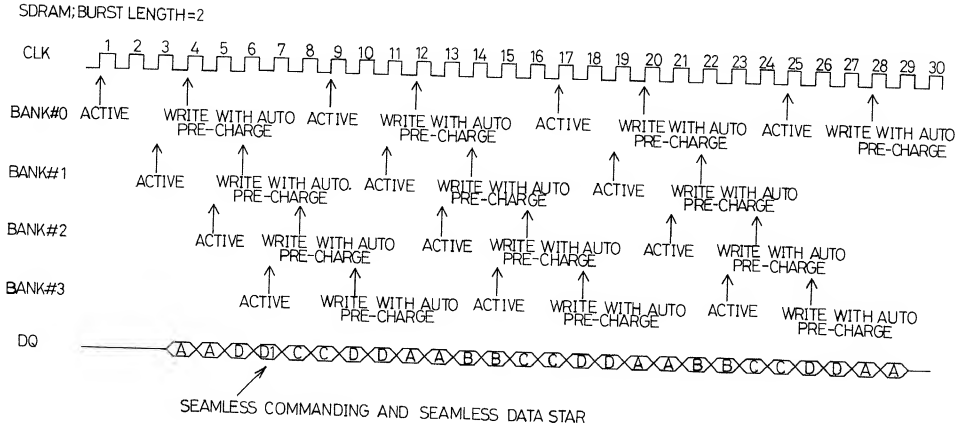

FIG.1A

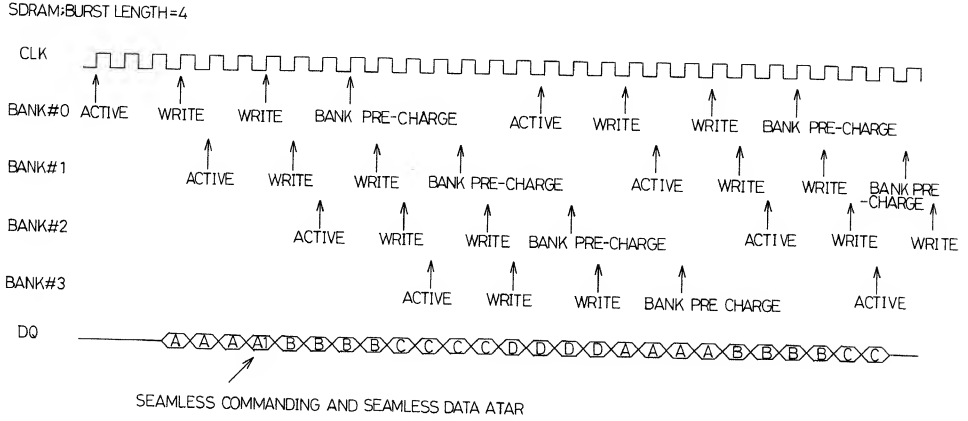

FIG.1B

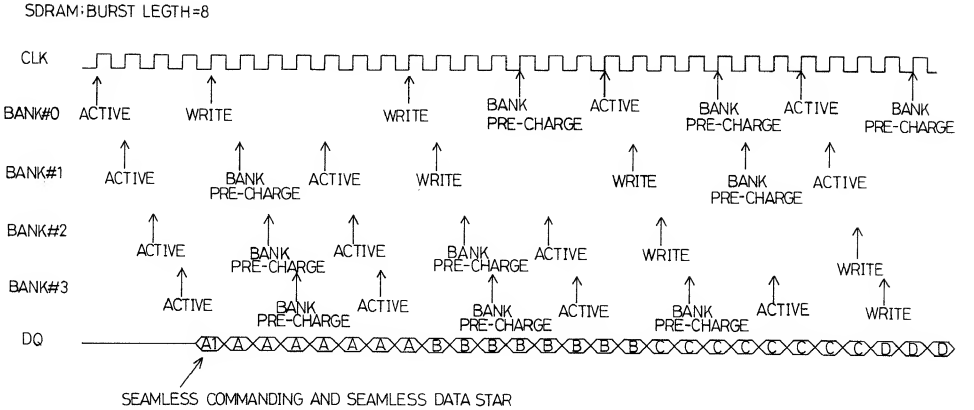

FIG.1C

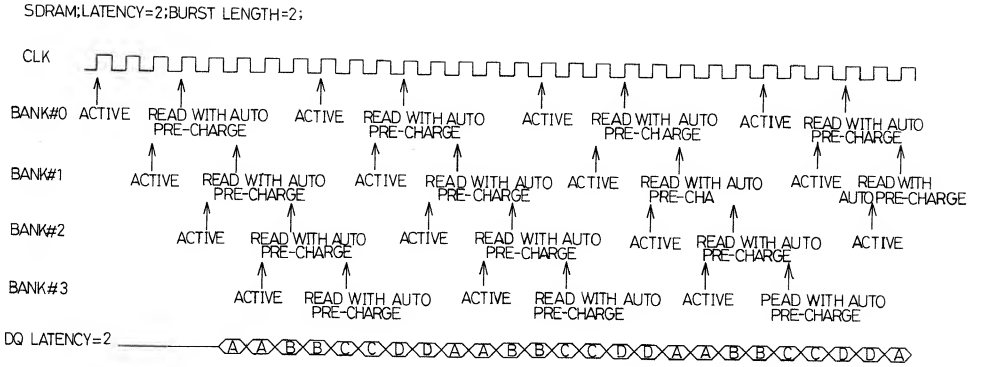

FIG. 2A

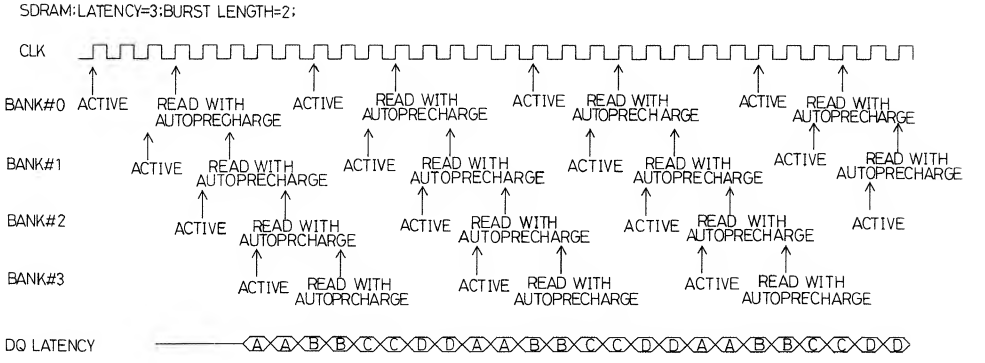

FIG. 2B

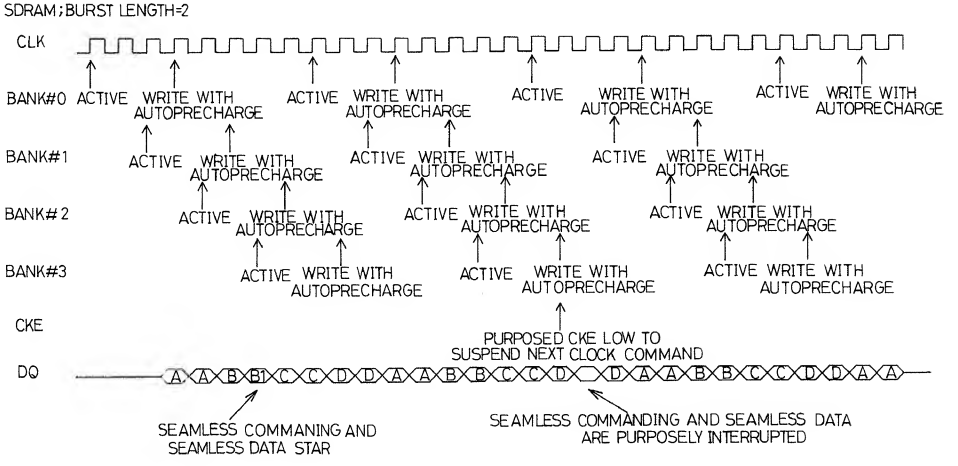

FIG.2C

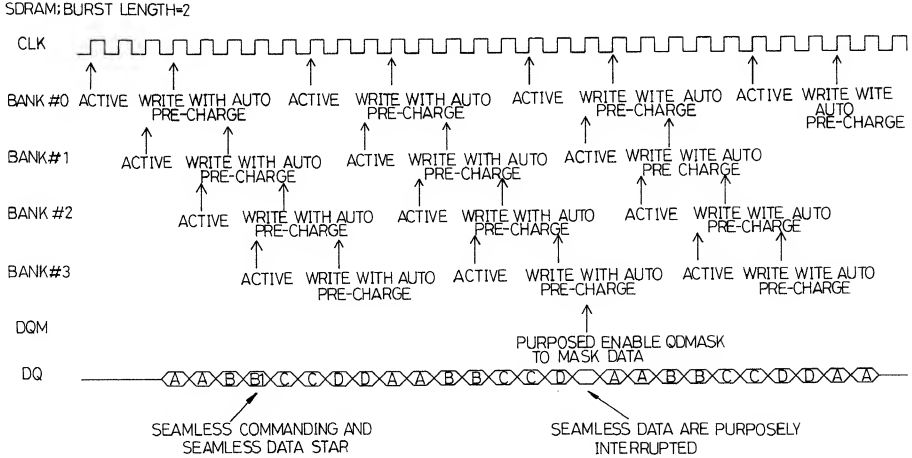
SDRAM; BURST LENGTH=2
CLK
BANK #0
BANK #1
BANK #2
BANK #3
DQM
DQ
ACTIVE
WRITE WITH AUTO PRE-CHARGE
WRITE WITE AUTO PRE-CHARGE
PURPOSED ENABLE QDMASK TO MASK DATA
SEAMLESS COMMANDING AND SEAMLESS DATA STAR
SEAMLESS DATA ARE PURPOSELY INTERRUPTED

FIG.2D

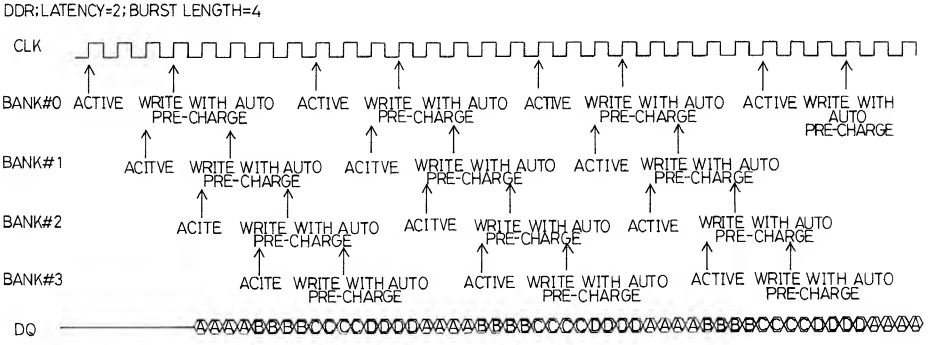

FIG.3A

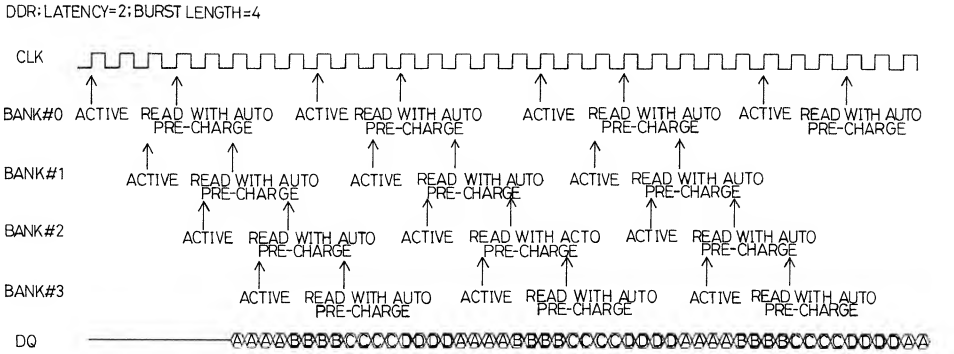
DDR: LATENCY=2; BURST LENGTH=4
CLK
BANK#0
BANK#1
BANK#2
BANK#3
DQ
ACTIVE
READ WITH AUTO PRE-CHARGE
READ WITH ACTO PRE-CHARGE

FIG.3B

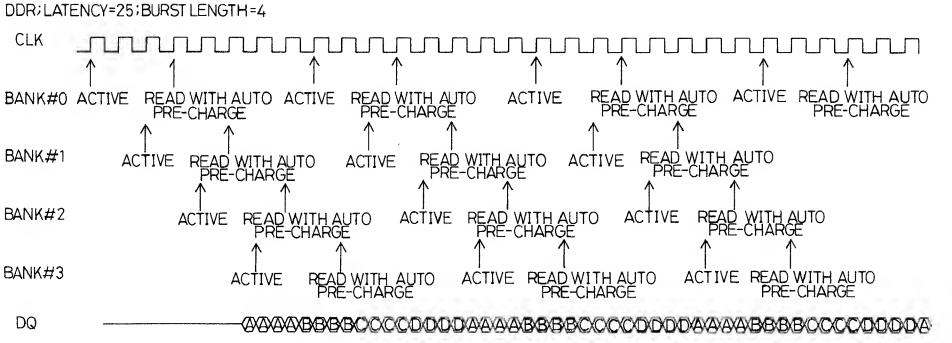

FIG.3C

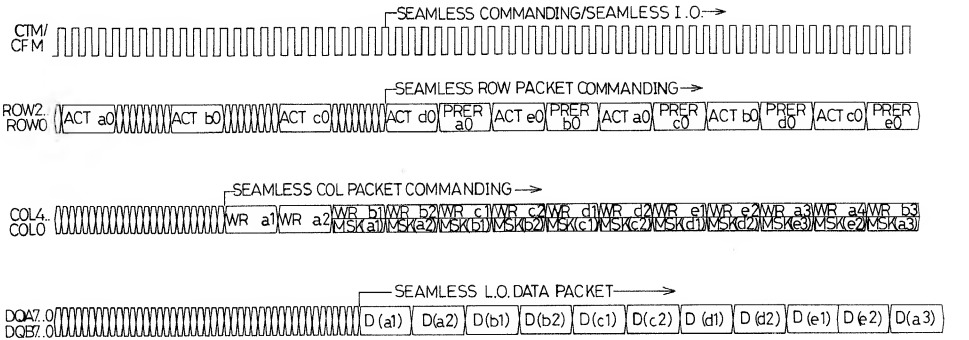

FIG.4A

TRANSACTION A:	a0={Da,Ba,Ra0}	a1={Da,Ba,Ca1}	a2={Da,Ba,Ca2}	a3={Da,Ba,Ca3}	a4={Da,Ba,Ca4}
TRANSACTION B:	b0={Db,Bb,Rb0}	b1={Db,Bb,Cb1}	b2={Db,Bb,Cb2}	b3={Db,Bb,Cb3}	b4={Db,Bb,Cb4}
TRANSACTION C:	c0={Dc,Bc,Rc0}	c1={Dc,Bc,Cc1}	c2={Dc,Bc,Cc2}	c3={Dc,Bc,Cc3}	c4={Dc,Bc,Cc4}
TRANSACTION D:	d0={Dd,Bd,Rd0}	d1={Dd,Bd,Cd1}	d2={Dd,Bd,Cd2}	d3={Dd,Bd,Cd3}	d4={Dd,Bd,Cd4}
TRANSACTION E:	e0={De,Be,Re0}	e1={De,Be,Ce1}	e2={De,Be,Ce2}	e3={De,Be,Ce3}	e4={De,Be,Ce4}

RDRAM: TRR=8 TCYCLE; TCAC=8 TCYCLE; TRAS=20 TCYCLE; TRDP=4 TCYCLE;

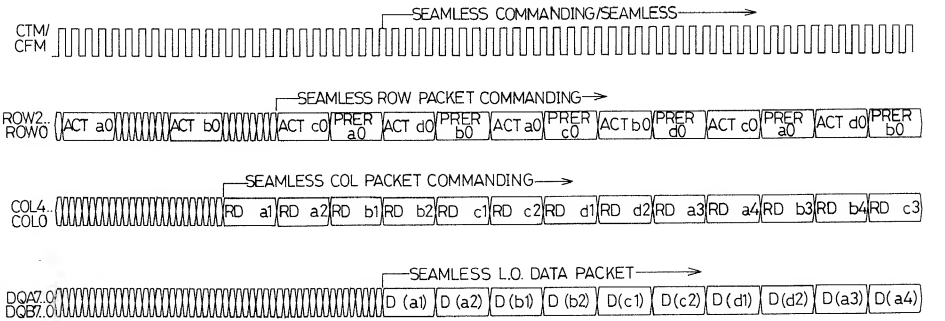

FIG.4B

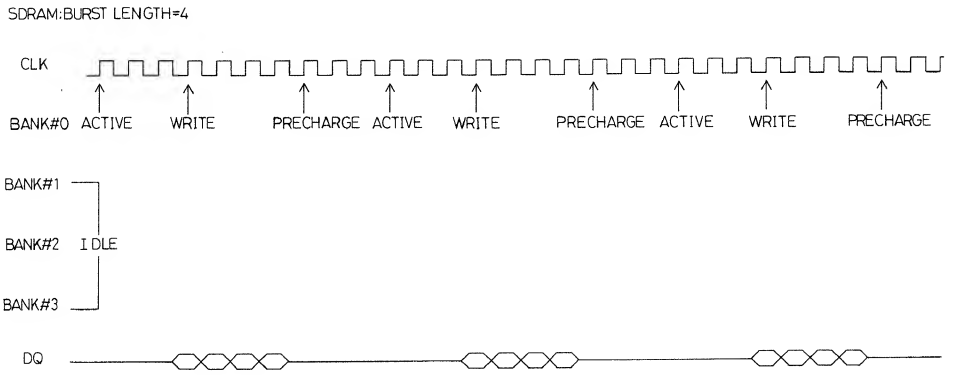

FIG.5
PRIOR ART

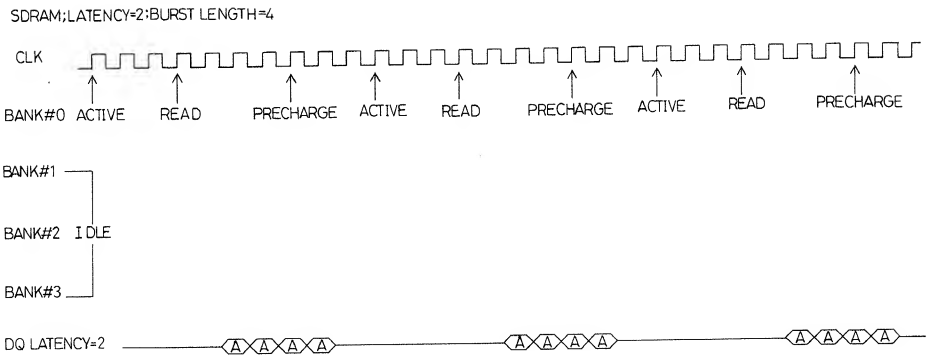

FIG.6A
PRIOR ART

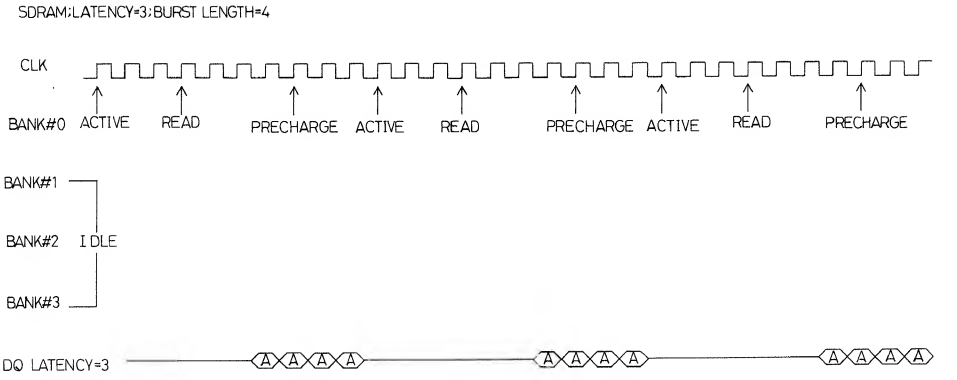

FIG.6B
PRIOR ART

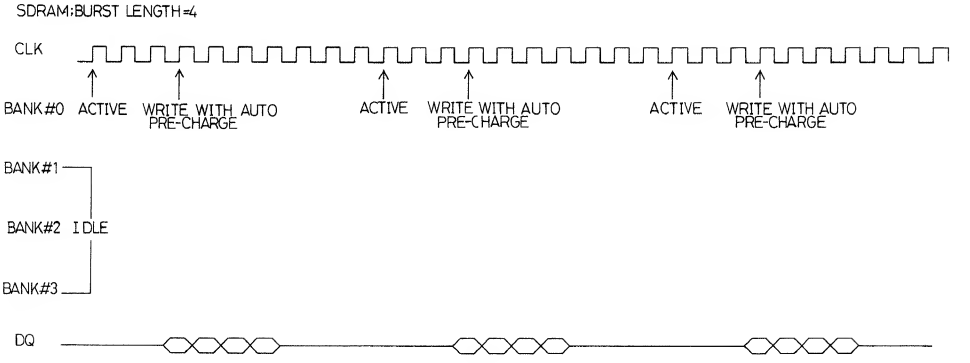

FIG.7
PRIOR ART

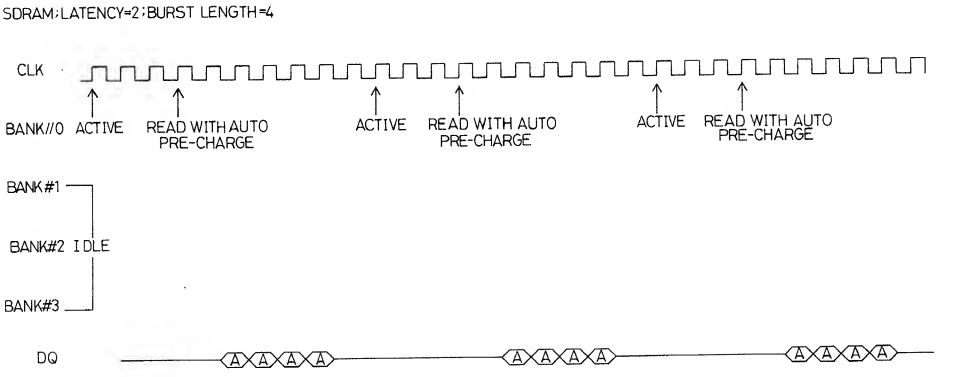

FIG.8A
PRIOR ART

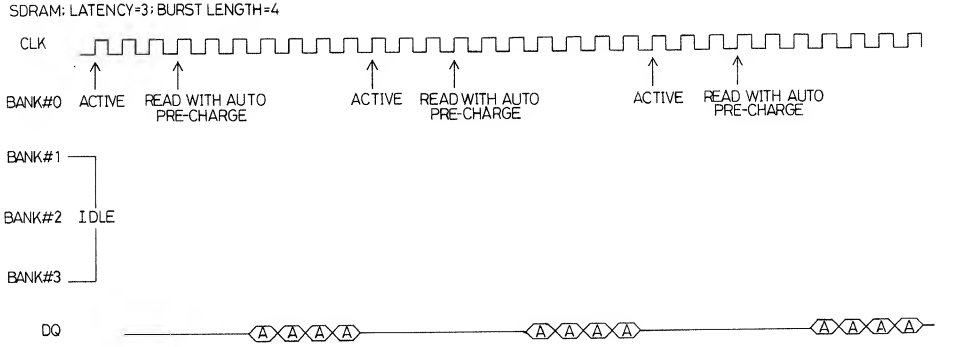

FIG.8B
PRIOR ART

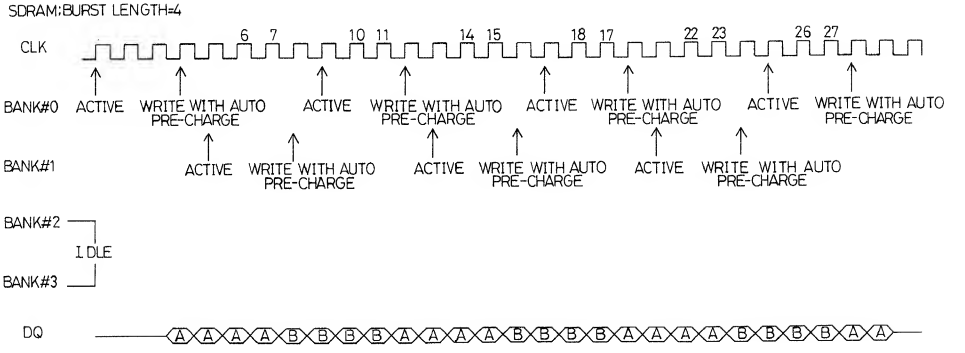

FIG.9
PRIOR ART

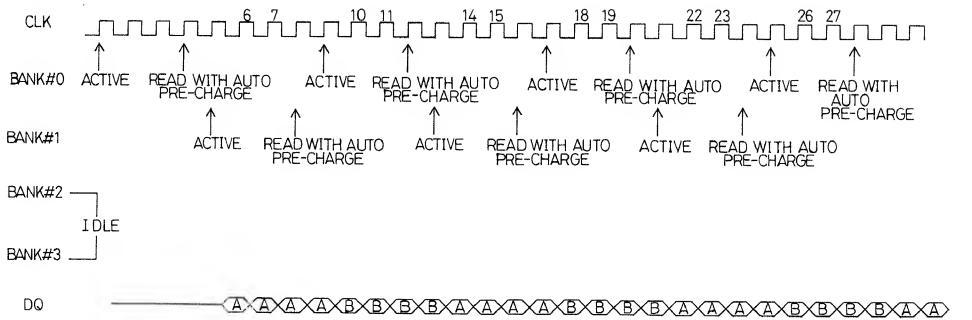

FIG.10A
PRIOR ART

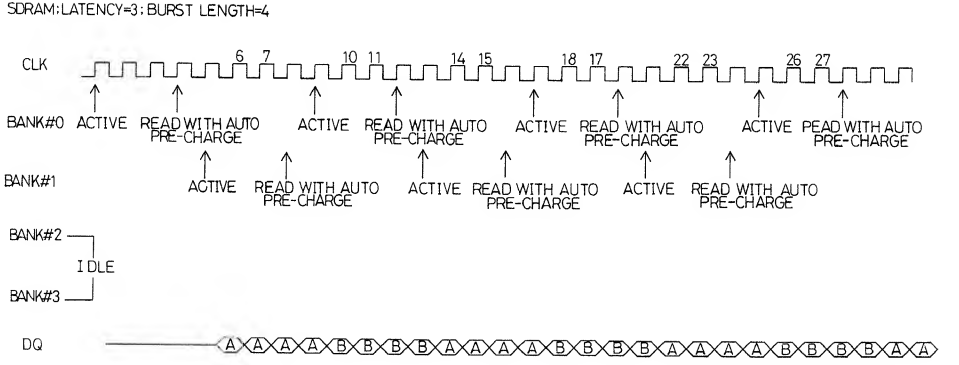

FIG.10B
PRIOR ART

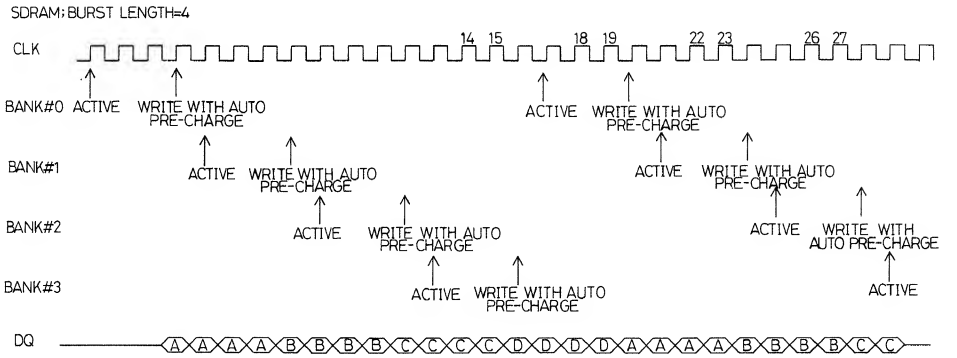

FIG.11
PRIOR ART

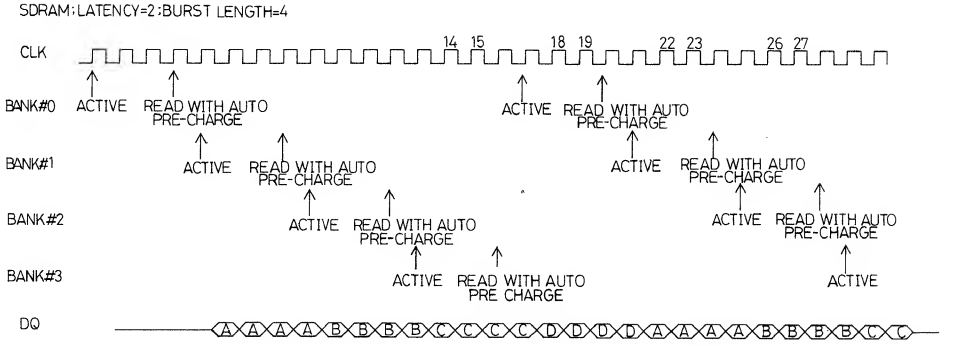

FIG.12A
PRIOR ART

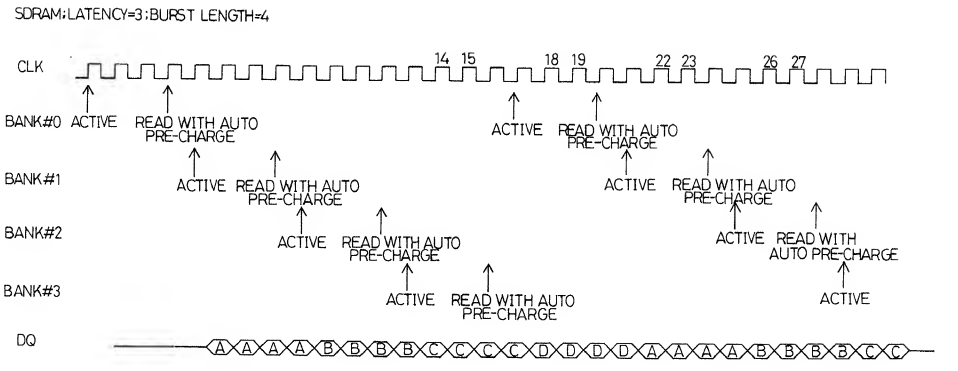

FIG.12B
PRIOR ART